



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:

Tam et al.

Serial No. 10/721,300

Filed: Nov. 24, 2003

For: Method and Pipeline  
Architecture for Processing  
Multiple Swap Requests to Reduce  
Latency

Examiner: LAI, V.

Art Unit: 2181

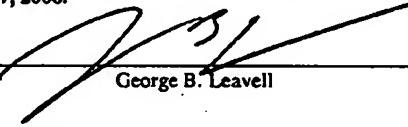
Atty Docket No. SUNMP351

Date: October 27, 2006

~~DO NOT ENTER~~  
*Entered Per RCE*  
*RWB 2-12-07*

**CERTIFICATE OF MAILING**

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on October 27, 2006.

Signed: 

George B. Leavell

**AMENDMENT AND RESPONSE TO OFFICE ACTION**

Commissioner for Patents  
Alexandria, VA 22313-1450

In response to the Office Action mailed August 28, 2006, please reconsider the above-referenced application as follows:

A complete listing of claims with their current status begins on page 2 of this paper.

Remarks begin on page 6 of this paper.